RESPONSE TO NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF

Applicant	:	Aggarwal et al.
App. No	:	10/665,693
Filed	:	09/17/2003
For	:	SYSTEM FOR THE IMPROVED HANDLING OF WAFERS WITHIN A PROCESS TOOL
Examiner	:	Gregory W. Adams
Art Unit	:	3652
Conf. No.	:	6237

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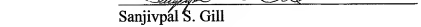
Sir:

This paper is submitted in response to the Notification of Non-Compliant Appeal Brief having a notification date of October 7, 2008 which relates to an Appeal Brief to the Board of Patent Appeals and Interferences filed September 12, 2008 in the above-captioned application.

The Notification indicates that the above-mentioned Appeal Brief does not include a notation of where in the record each incidence of evidence appeared.

In response, the Applicants submit the entire corrected brief and attach hereto a copy of U.S. Patent No. 6,073,366 to Aswad. The corrected "Evidence Appendix" now contains a notation of where in the record Aswad first appeared. In light of the corrected brief and the copy of U.S. Patent No. 6,073,366 to Aswad attached hereto, the Applicants respectfully submit that this paper is fully responsive to the Notification mailed October 7, 2008. The Applicants submit that the above-mentioned Appeal Brief is now in compliance with the provisions of 37 CFR 41.37.



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APPEAL BRIEF

Sir:

This Appeal Brief relates to an appeal to the Board of Patent Appeals and Interferences of the rejections set forth in the Final Office Action having a notification date of April 15, 2008 in the above-captioned application.

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I. REAL PARTY IN INTEREST

The real party in interest in this appeal is the assignee of this application, ASM AMERICA, INC.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeals or interferences.

III. STATUS OF CLAIMS

Claims 1–23 are currently pending and are the subject of this Appeal as all of these claims are rejected under a variety of grounds as detailed below. The independent claims are Claims 1, 10, and 14. The claims are attached hereto in the Claims Appendix, Section VIII.

IV. STATUS OF AMENDMENTS

The claims before the Board appear as they were finally rejected in the Final Office Action mailed April 15, 2008.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The disclosed embodiments relate generally to a buffer station configured to provide a less contaminated inert internal environment as compared with the internal environment of a cassette docked to the docking port (*see, e.g.,* ¶ 0008 of the Specification). The buffer station also has a rack with multiple shelves for holding substrates (Specification, ¶ 0008). In some embodiments, the buffer stations employ racks having reduced pitch between the shelves, allowing the volume of a buffer station to be reduced in order to allow the station to be more quickly purged (Specification,¶ 0032). This allows the buffer station to be closed and purged in order to create an inert environment in which to store the substrates, free of the moisture and oxygen of the clean room environment in order to minimize oxidation or other contamination of the substrates while they await processing (Specification,¶ 0056). Support for each independent claim is provided below, with reference to the specification and drawings. Reference numerals for corresponding elements of the specification and drawings are provided for ease of understanding. However, it should be understood that the claimed invention is not limited to the disclosed and described embodiments.

Claim 1 recites, with reference to **FIGS. 1, 3–4** and ¶¶ 42–48:

1. A semiconductor processing tool comprising:

a first substrate handling chamber **22**;

a front docking port **14** located on an outside surface of the first substrate handling chamber **22**;

a robot arm **24** located in the first substrate handling chamber **22**;

a loadlock chamber **40** joined to the first substrate handling chamber **22**; and

a buffer station **30** directly adjacent the first substrate handling chamber **22** and separate from the loadlock chamber **40**, the buffer station **30** being purged with an inert internal environment separate from the first substrate handling chamber **22**, the buffer station **30** having a rack **38** defining multiple shelves for holding substrates;

wherein the robot arm **24** is configured to access the buffer station **30**.

Claim 10 recites, with reference to **FIGS. 1, 3–4** and ¶¶ 42–48:

10. A semiconductor processing tool in combination with a front opening unified pod (FOUP) cassette, comprising:

a FOUP cassette **10** including multiple shelves **18** for holding substrates of a particular size;

a first substrate handling chamber **22**;

a front docking port **14** located on the outside surface of the first substrate handling chamber **22**;

a robot arm **24** located in the first substrate handling chamber **22**;

a loadlock chamber **40** joined to the first substrate handling chamber **22**; and

a buffer station **30** directly adjacent the first substrate handling chamber **22** and separate from the loadlock chamber **40**, the buffer station **30** being purged with an inert internal environment separate from the first substrate handling chamber **22**, the buffer station **30** having a rack defining multiple shelves **18** for holding substrates of said particular size, wherein the shelves **18** of the buffer station **30** rack have a reduced pitch relative to the shelves of the FOUP cassette **10**;

wherein the robot arm **24** is configured to access the buffer station **30**.

Claim 14 recites, with reference to **FIGS. 1, 3–4** and ¶¶ 42–48:

14. A semiconductor processing tool comprising:

a substrate handling chamber **22**;

a front docking port **14** located on an outside surface of the substrate handling chamber **22**, the port **14** being capable of mating with a substrate cassette;

a purgeable buffer station **30** joined with the substrate handling chamber **22** such that it is possible to transfer substrates directly between the substrate handling chamber **22** and the buffer station **30**, the purgeable buffer station configured for sealing and separately purging from the substrate handling chamber **22**, the buffer station **30** being located in position downstream of the front docking port **14**, the buffer station **30** having only one opening for substrate transfer to and from the buffer station **30**; and

a buffer station rack within the buffer station **30** being configured to have multiple slots **18** for holding substrates.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The Examiner has rejected independent Claims 1, 10, and 14 as well as all claims that depend from them, under 35 U.S.C. 103(a) as being obvious over Hofmeister (U.S. Pat. No. 6,481,956, hereinafter "Hofmeister") in view of Tanaka (U.S. Pat. No. 6,395,094, hereinafter "Tanaka") and further in view of Ozawa et al. (U.S. Pat. No. 5,810,538, hereinafter "Ozawa").

VII. ARGUMENT

A. Disclosure of Hofmeister, Tanaka, and Ozawa

Hofmeister discloses, in Figure 2, an apparatus including cassette load ports **26** for receiving substrate cassettes or capsils **34**. The apparatus further includes a cassette stocker **24**, substrate cassette pod door removers **28**, a loading section **13**, a substrate transport robot **32** within the loading section **13**, and load locks **16** connected to the loading section **32**. The loading section **13** contains four buffer cassettes **B1-B4**. Hofmeister teaches using the buffer cassettes **B1-B4** as temporary substrate storage locations within the loading section **13**, and states that "[t]he buffers may be eliminated if there is no pre or post align or if repeated capsil access is acceptable." Col. 3, lines 28-39.

Tanaka discloses, in Figure 1a, a process system including wafer cassette housing chambers **30A** and **30B**, a transfer chamber **28**, process chambers **26A-D**, and buffer parts **44** and **46**. A system **100** supplies the transfer chamber **28** and cassette housing chambers **30A** and **30B** with an inert gas, such as N_2, and these chambers are also provided with a vacuum exhaust system **102**. Col. 7, lines 51-54. Referring to Figures 2-5, each buffer part **44, 46** includes a single-wafer preheating unit **48** and a single-wafer cooling unit **50**. Each buffer part **44, 46** can be airtightly separated from the transfer chamber **28** during wafer preheating or cooling. The cooling unit **50** includes a cooling gas system **94** for selectively introducing a cooling gas, such as a cooled N_2 gas, and an exhaust system **96** connected to a vacuum pump or the like for discharge of the cooling gas. Col. 7, lines 36-44.

Ozawa discloses, in Figure 1, semiconductor manufacturing equipment comprising an enclosure **37** having a front shutter **38**. A multi-shelf cassette stocker **24** is positioned for transferring, via a vertically movable cassette transfer unit **40**, cassettes **26** to/from a cassette stage **39**, which is adjacent the front shutter **38**. The tool also comprises a reaction chamber **15**, a load-lock chamber **17**, and a boat elevator **30** for loading and unloading a boat **18** to and from the reaction chamber **15**. A carrying elevator **22** is face-to-face with the boat elevator **30**. The carrying elevator **22** is provided with a wafer carrier **23** (for transferring as many wafers as desired from the boat elevator **18** to the cassette stocker **24**), and a wafer holder (not shown) is

designed such that its pitch can be adjusted to match either the pitch of the wafers held within the wafer cassettes **26** or the pitch of the wafers held within the boat **18**. Ozawa, col. 4, lines 45-50.

B. Legal Requirements for Establishing a Showing of Obviousness

In an obviousness rejection based on a combination of references, the claimed invention "is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *KSR International Co. v. Teleflex Inc., et al.*, 127 S.Ct. 1727, 1741 (2007). "[I]t can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does." *Id.* It will often "be necessary ... to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue. To facilitate review, this analysis should be made explicit." *Id.* at 1740-41.

Also, to establish a *prima facie* case of obviousness, there must be a reasonable expectation of success for a proposed modification of a prior art reference. M.P.E.P. § 706.02(j); *In re Vaeck*, 947 F.2d 488, 493 (Fed. Cir. 1991).

C. Obviousness over Hofmeister in View of Tanaka and Ozawa

1. The Examiner Has Provided No Convincing Reason to Combine Hofmeister with Tanaka to Form the Limitations of Claims 1, 10, or 14

In its rejection, the Final Office Action dated April 15, 2008 points to Hofmeister's loading section **13** and buffer cassettes B1-B4 as the claimed "substrate handling chamber" and "buffer station," respectively. With regard to the claimed limitation that "the buffer station [is] purged with an inert internal environment separate from the first substrate handling chamber," the Office Action points to Tanaka's cooling gas system **94** of the buffer stations **44** and **46**. In particular, the Office Action refers to Tanaka's teaching of airtightly separating the buffer station **44**, **46** from the transfer chamber **28** during wafer preheating or cooling "to prevent a gas, which has been released or exhausted from the surface of the object during preheating, and a cooling gas, which has been used for cooling, from being leaked into the transfer chamber." Tanaka, col. 3, lines 43-47. The Office Action indicates that it would have been obvious to modify one of

Hofmeister's buffer cassettes **B1**-**B4** to comprise a buffer station directly adjacent the loading section **13**, and to purge the buffer station with an inert internal environment separate from the loading section **13**, "as per the teachings of Tanaka, to contain leakage into a transfer chamber." Office Action, page 4. It is necessary for the Examiner, in supporting his *prima facie* case of obviousness, to articulate some reason that one of ordinary skill in the art would have been led to the presently claimed invention in view of the prior art.[1] However, the Examiner's asserted reason for combining, "to contain leakage into a transfer chamber," is inconsistent with the teachings of both Hofmeister and Tanaka.

The purported reason given by the Examiner is unconvincing because Hofmeister's buffer cassettes **B1-B4** are present in the ambient environment of the substrate loading section **13** (asserted by the Examiner to be equivalent to the transfer chamber **28** of Tanaka). Since Hofmeister's buffer cassettes **B1-B4** are present in the ambient environment, and Hofmeister does not express any concern that "leakage" from the buffer cassettes to the ambient environment be contained, one of ordinary skill in the art would have had no reason to make the combination. As understood by one of ordinary skill in the art, Hofmeister's buffer cassettes **B1-B4** merely temporarily hold substrates in the ambient environment of the loading section **13** until they are then moved for further processing. Indeed, "contain[ing] leakage" only becomes an issue in Tanaka, since Tanaka teaches pre-heating or cooling wafers in the buffer part **44** before or after processing. Only during the pre-heating or cooling would one of ordinary skill in the art seek to "contain leakage." Thus Tanaka creates a problem (by seeking to heat or cool wafers), then solves it (using the sealed buffer part **44**). Hofmeister does not indicate the need to pre-heat or cool wafers, nor that "leakage" from the wafers in the buffer cassette **B1-B4** needs to be "contained." Leakage is only a problem when one seeks to prevent gas flow from one compartment to another. Hofmeister does <u>not</u> seek to prevent gas flow from the buffers **B1-B4** to the remainder of the loading section **13**. Given the teachings of the two references, one of

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[1] *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d 1385 (2007). The key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious. The Supreme Court noted that the analysis supporting a rejection under 35 U.S.C. 103 should be made explicit.

ordinary skill would have had no reason to modify the buffer cassettes **B1-B4** of Hofmeister to be purgeably separate from the substrate loading section **13**.

In response, the Examiner states that "[w]hether a modifying reference solves a problem explicitly noted in a primary reference is irrelevant. The question is whether one skilled in the art would have combined the references together." (Final Office Action, dated April 15, 2008, page 6). It is true that the question is whether one skilled in the art would have combined the references together as the Examiner has stated, however, whether a modifying reference solves a problem is relevant to the question of whether one skilled in the art would have combined the references. As such, since Hofmeister's buffer cassettes **B1-B4** are in the ambient environment of the loading section **13**, Hofmeister simply has no leakage problem. Since the reason cited by the Examiner is one peculiar only to the Tanaka reference, one of ordinary skill in the art would not have had any reason to modify Hofmeister's buffer cassettes **B1-B4** as asserted by the Examiner.

2. <u>One of Ordinary Skill in the Art Would Not Have Modified the Buffer Cassette of Hofmeister in View of the Buffer Part of Tanaka</u>

As noted in the previous section, one of ordinary skill in the art would not have had any reason to combine the references as the Examiner has asserted. Indeed, had one of ordinary skill in the art sought to modify Hofmeister in view of Tanaka's teachings, he or she would have <u>added</u> Tanaka's single-wafer buffer part to Hofmeister's apparatus to pre-heat a wafer or conduct post-process cooling of a wafer. However, such a modification of Hofmeister would not have produced the limitations of Claims 1, 10, and 14, which involve a purged buffer station for multiple substrates.

Tanaka teaches that buffer part **44, 46** can be used for "housing therein the wafer W from the transfer chamber **28** during the preheating or cooling of the wafer." (Tanaka, column 6, lines 35-37). On the other hand, the purpose of the buffer cassettes **B1-B4** of Hofmeister is to temporarily hold substrates while they await further processing downstream from the transfer chamber. Therefore, one of ordinary skill in the art would have combined the teachings of the two references, if at all, by taking the apparatus of Hofmeister, and adding to it the buffer part of Tanaka, not, as the Examiner suggests, by modifying Hofmeister's buffer cassettes to be capable

of "being purged with an inert internal environment separate from the first substrate handling chamber[.]" Hence, one of ordinary skill in the art would not have produced the limitations of Claim 1, 10, and 14 in view of the teachings of the two references, and the claims are therefore not obvious.

3. <u>One Having Ordinary Skill in the Art Would Not Have Had a Reasonable Expectation of Success in Combining Hofmeister with Tanaka in the Manner Asserted by the Examiner</u>

The Examiner asserts that the combination of Hofmeister and Tanaka would have led one of ordinary skill in the art to the limitation of Claims 1 and 10 of "the buffer station being purged with an inert internal environment separate from the first substrate handling chamber" and the limitation of Claim 14 of "the purgeable buffer station configured for sealing and separately purging from the substrate handling chamber[.]" However, one of ordinary skill in the art would have had no reasonable expectation of success in the combination given the teachings of Tanaka. The person of skill would therefore not have been led to the limitations of Claims 1, 10, and 14.

Each of Claims 1, 10, and 14 requires that the buffer station be capable of holding multiple substrates. Claims 1 and 10 both recite "the buffer station having a rack defining multiple shelves for holding substrates" and Claim 14 recites "a buffer station rack within the buffer station being configured to have multiple slots for holding substrates." Hence, for any of Claims 1, 10, or 14 to be obvious over the combination of Hofmeister and Tanaka, one of ordinary skill in the art must have had a reasonable expectation of success for cooling multiple hot substrates in a cassette rack. But this is simply not the case, as explained below.

Tanaka teaches the use of a buffer part to separately preheat and cool down a single wafer before and after processing. As mentioned in Tanaka, after processing, a wafer may be about 600°C. (Tanaka, column 9, lines 5–10). Since the single wafer may be at such an elevated temperature, Tanaka teaches the use of supporting pins **90** to support the hot wafer in the buffer part. (Tanaka, column 6, lines 58–62). As generally known in the art, such pins are typically formed of a material capable of withstanding very high temperatures, so that they can be used during the cooling of a hot wafer. Tanaka's supporting pins **90** are not capable of supporting multiple wafers.

In contrast, each of Hofmeister's buffer cassettes **B1-B4** holds multiple substrates. Hofmeister does not describe the material properties of the buffer cassettes **B1-B4**. Nor does Hofmeister disclose cooling wafers within the buffer cassettes **B1-B4**. Therefore, skilled artisans would have interpreted Hofmeister's buffer cassettes **B1-B4** as conventional cassette racks designed to hold substrates at ambient temperatures. Conventional cassette racks are not designed to receive hot wafers or to hold hot wafers during substrate cooling. For example, U.S. Patent No. 6,073,366 to Aswad[2] states:

> "Because of the high temperature CVD processing, transport from the process chamber directly to a wafer cassette is not possible due to the temperature of the wafer exceeding the material properties of most commonly used cassette materials. Because of this, the transfer of the wafer to a cassette must be postponed until the wafer temperature falls below the thermal properties of the cassette material. While cassettes are available that can handle wafers as hot as 170°C., they are relatively expensive. A commonly available less expensive one made of Delrin® can only handle temperatures well below 100°C. Other commonly available units can only handle about 60°C."

Aswad, col. 1, lines 25-38. Thus, it was understood that cassette racks cannot be used to cool substrates that are hotter than 170°C. Therefore, skilled artisans would not have had a reasonable expectation of success for the Office Action's proposed modification of Hofmeister's buffer cassettes **B1-B4** to act as substrate cooling stations. Appellants respectfully assert that had the skilled artisan desired to provide a substrate cooling station in Hofmeister, he or she would have opted to provide a ***single-substrate*** cooling station (such as Tanaka's cooling unit **50**) ***in addition to*** the buffer cassettes **B1-B4**, as opposed to converting one of the buffer cassettes **B1-B4** into a cooling station.

In response to this, the Examiner argues that "[w]hether Hoffmeister's [*sic*] apparatus could handle extreme cooling or heating is irrelevant because claims 1-23 do not specifically call for said features[.]" It is true that Claims 1–23 do not require features of handling extreme cooling or heating, however, whether Hofmeister's buffer cassettes could handle extreme cooling or heating (as does Tanaka's buffer part) is relevant to the question of whether one of ordinary

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[2] A copy of U.S. Patent No. 6,073,366 to Aswad is submitted herewith for the Board's convenience.

skill in the art would have had a reasonable expectation of success in combining the teachings of two references. The Examiner's counterargument misses the focus of Appellants' argument and plainly disregards the expectation of success requirement.

4. Ozawa Does Not Cure the Defects in the Asserted Hofmeister-Tanaka Combination

Ozawa is cited merely for its teachings related to a reduced pitch between an origination and destination (Final Office Action, dated April 15, 2008, page 4) and does not cure the defects discussed above in Hofmeister and Tanaka. The Office Action cites Ozawa for assertedly making it obvious to store substrates in a buffer station at a reduced pitch relative to a FOUP. First, this aspect of Ozawa is irrelevant to independent Claims 1 and 14, neither of which recites a reduced pitch buffer station. Second, with respect to independent Claim 10, Ozawa does not actually make it obvious to store substrates in a buffer station at a reduced pitch. Ozawa merely discloses a wafer holder designed such that its pitch can be adjusted to match either the pitch of a wafer cassette or the pitch of a wafer boat. Ozawa, col. 4, lines 45-50. Thus, while Ozawa might have suggested modifying Hofmeister to include an adjustable-pitch substrate holder, it would not have suggested modifying the pitch of Hofmeister's buffer cassettes **B1-B4**.

D. CONCLUSION

Each of Appellant's independent claims recites a buffer station being purged or purgeable separately from a substrate handling chamber, where the buffer station has a rack capable of holding multiple substrates. Contrary to the Examiner's assertions, the claimed inventions are not obvious because one of ordinary skill in the art armed with the teachings of the cited references would not have had any reason to make the asserted combination, would have made a different combination for a different reason, and would not have had a reasonable expectation of success. Claims 1, 10, and 14 are therefore not obvious in view of the cited art.

Respectfully Submitted,

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VIII. CLAIMS APPENDIX

1. **(Previously presented)** A semiconductor processing tool comprising:

a first substrate handling chamber;

a front docking port located on an outside surface of the first substrate handling chamber;

a robot arm located in the first substrate handling chamber;

a loadlock chamber joined to the first substrate handling chamber; and

a buffer station directly adjacent the first substrate handling chamber and separate from the loadlock chamber, the buffer station being purged with an inert internal environment separate from the first substrate handling chamber, the buffer station having a rack defining multiple shelves for holding substrates;

wherein the robot arm is configured to access the buffer station.

2. **(Original)** The semiconductor processing tool according to Claim 1, wherein the rack is configured to support a plurality of 300 mm silicon wafers.

3. **(Original)** The semiconductor processing tool according to Claim 1, further comprising a rear substrate handling chamber, where the loadlock chamber is located between the first substrate handling chamber and the rear substrate handling chamber.

4. **(Original)** The semiconductor processing tool according to Claim 1, wherein the buffer station is further configured to create an inert environment which is selectively isolated from the first substrate handling chamber.

5. **(Original)** The semiconductor processing tool according to Claim 4, wherein the buffer station is further configured to be selectively purged.

6. **(Original)** The semiconductor processing tool according to Claim 4, wherein the buffer station rack is configured to allow the robot arm to be capable of accessing the entire buffer station rack through the use of a z-motion of the robot arm.

7. **(Previously presented)** The semiconductor processing tool according to Claim 1, wherein the buffer station is configured to have an internal volume less than or equal to about 18.3 liters.

8. **(Original)** The semiconductor processing tool according to Claim 7, wherein the buffer station rack is configured to support twenty-five 300 mm silicon wafers.

9. **(Previously presented)** The semiconductor processing tool according to Claim 1, wherein the loadlock chamber is configured to have an internal volume less than or equal to about 9.156 liters.

10. **(Previously presented)** A semiconductor processing tool in combination with a front opening unified pod (FOUP) cassette, comprising:

a FOUP cassette including multiple shelves for holding substrates of a particular size;

a first substrate handling chamber;

a front docking port located on the outside surface of the first substrate handling chamber;

a robot arm located in the first substrate handling chamber;

a loadlock chamber joined to the first substrate handling chamber; and

a buffer station directly adjacent the first substrate handling chamber and separate from the loadlock chamber, the buffer station being purged with an inert internal environment separate from the first substrate handling chamber, the buffer station having a rack defining multiple shelves for holding substrates of said particular size, wherein the shelves of the buffer station rack have a reduced pitch relative to the shelves of the FOUP cassette;

wherein the robot arm is configured to access the buffer station.

11. **(Previously presented)** The semiconductor processing tool and FOUP cassette according to Claim 10, wherein the robot arm is configured to employ a variable pitch end effector having multiple end effector shelves.

12. **(Previously presented)** The semiconductor processing tool and FOUP cassette according to Claim 10, wherein the first substrate handling chamber is configured to operate at atmospheric pressure.

13. **(Previously presented)** The semiconductor processing tool and FOUP cassette according to Claim 10, wherein the first substrate handling chamber is configured to operate at reduced pressure.

14. **(Previously presented)** A semiconductor processing tool comprising:

a substrate handling chamber;

a front docking port located on an outside surface of the substrate handling chamber, the port being capable of mating with a substrate cassette;

a purgeable buffer station joined with the substrate handling chamber such that it is possible to transfer substrates directly between the substrate handling chamber and the buffer station, the purgeable buffer station configured for sealing and separately purging from the substrate handling chamber, the buffer station being located in position downstream of the front docking port, the buffer station having only one opening for substrate transfer to and from the buffer station; and

a buffer station rack within the buffer station being configured to have multiple slots for holding substrates.

15. **(Previously presented)** The semiconductor processing tool according to Claim 14, in combination with a substrate cassette mated with the port, the substrate cassette having a cassette rack, the processing tool further comprising a loadlock chamber joined with the substrate handling chamber, the loadlock chamber having a loadlock rack with a substrate capacity of less than one third of a substrate capacity of the cassette.

16. **(Original)** The semiconductor processing tool according to Claim 15, further comprising a rear substrate handling chamber where the loadlock chamber is located between the substrate handling chamber and the rear substrate handling chamber.

17. **(Original)** The semiconductor processing tool according to Claim 15, wherein the substrate capacity of the loadlock chamber is 1 to 7 substrates.

18. **(Original)** The semiconductor processing tool according to Claim 15, wherein the loadlock rack is configured to support a plurality of 300 mm silicon wafers.

19. **(Original)** The semiconductor processing tool according to Claim 14, wherein the substrate handling chamber is configured to operate at standard atmospheric pressure.

20. (**Original**) The semiconductor processing tool according to Claim 14, wherein the substrate handling chamber is configured to operate at reduced pressure.

21. **(Previously presented)** The semiconductor processing tool according to Claim 14, in combination with a substrate cassette mated with the port, the substrate cassette having a cassette rack, wherein the buffer station rack has a reduced relative spacing between the rack slots as compared with a relative spacing between slots of the cassette rack.

22. **(Previously presented)** The semiconductor processing tool according to Claim 21, wherein the buffer station rack is configured to allow a robot arm to access the entire buffer station rack through the use of a robot arm's z-motion.

23. **(Previously presented)** The semiconductor processing tool according to Claim 14, in combination with a substrate cassette mated with the port, the substrate cassette having a cassette rack with multiple slots for holding substrates, the processing tool further comprising a robot arm configured to have a variable pitch end effector designed to transfer multiple substrates from the cassette rack to the buffer station rack, the cassette rack having unequal slot pitch relative to the buffer station rack.

IX. EVIDENCE APPENDIX

Attached hereto is a copy of U.S. Patent No. 6,073,366 to Aswad. Appellants first raised the import of the Aswad patent on the last line of page 9 of the Amendment filed March 3, 2008, responding to the Office Action of December 3, 2007. Additionally, Appellants submitted a copy of the Aswad patent along with the Amendment of March 3, 2008.

X. RELATED PROCEEDINGS APPENDIX

No related appeal proceedings are known.